

Table of Contents

	<u>Page</u>
Preface	
Table of Contents.....	i
List of Figures.....	v
List of Tables	ix
I Scope	1
II Handbook Introduction.....	2
1 Electronic System Reliability Prediction.....	3
1.1 History of Reliability Prediction Methods.....	3
1.1.1 Electronic Reliability Prediction Methods	5
1.2 Reliability Criteria	14
1.2.1 The Failure Rate Curve for Electronic Systems	15
1.2.2 Basic Lifetime Distribution Models	17
1.3 Reliability Testing	21
1.3.1 Reliability Test Methods	22
1.3.2 Accelerated Testing	27
1.4 Bibliography	31
2 New Physics-of-Failure Based Circuit Reliability/Methodology	33
2.1 Introduction	33
2.2 Problematic Areas.....	34
2.2.1 Zero Failure Criteria	34
2.2.2 Single Failure Mechanisms vs. Competing Failure Mechanisms	38
2.2.3 Accelerated Factors	40
2.2.4 Electronic-System Constant-Failure-Rate Approximation/ Justification.....	53
2.3 Physics-of-Failure Based Circuit Reliability Prediction Methodology.....	63
2.3.1 Introduction	63
2.3.2 Methodology.....	65
2.4 Bibliography	78
3 Failure Mechanisms.....	83
3.1 Introduction and Classification.....	83
3.2 Time Dependent Dielectric Breakdown	86
3.2.1 Introduction	86

Table of Contents (continued)

	<u>Page</u>
3.2.2	Physics of Breakdown 86
3.2.3	Early Models for Dielectric Breakdown..... 89
3.2.4	Acceleration Factors 90
3.2.5	Models for Ultra-Thin Dielectric Breakdown 91
3.2.6	Statistical Model 94
3.3	Hot Carrier Injection..... 95
3.3.1	Introduction 95
3.3.2	Hot-Carrier Effects 96
3.3.3	Hot Carrier Generation Mechanism and Injection to the Gate Oxide Film 97
3.3.4	Hot Carrier Models 100
3.3.5	Hot Carrier Degradation 102
3.3.6	Hot Carrier Resistant Structures 106
3.3.7	Acceleration Factor..... 107
3.3.8	Statistical Models for HCI lifetime 107
3.3.9	Lifetime Sensitivity 108
3.4	Negative Bias Temperature Instability 109
3.4.1	Introduction 109
3.4.2	Physics-of-Failure..... 109
3.4.3	Interface Trap Generation: Reaction -Diffusion Model 110
3.4.4	Fixed Charge Generation..... 112
3.4.5	Recovery and Saturation..... 112
3.4.6	NBTI Models..... 113
3.5	Electromigration 114
3.5.1	Introduction 114
3.5.2	EM Physics..... 115
3.5.3	Lifetime Prediction 117
3.5.4	Lifetime Distribution Model..... 118
3.5.5	Lifetime Sensitivity 118
3.6	Soft Errors Due to Memory Alpha Particles 119
3.6.1	Soft Error Model..... 119
3.7	Bibliography 120
4	Failure Mechanisms and Reliability Modeling of Electronic Packages 127
4.1	Introduction 127
4.1.1	Electronic Package Systems 127
4.1.2	Reliability of Electronic Packages..... 129
4.2	Failure Mechanisms of Electronic Packages 132

Table of Contents (continued)

	<u>Page</u>
4.2.1 Introduction	132
4.2.2 Failure Mechanisms and Model Descriptions	138
4.3 Reliability Prediction of Electronic Packages	171
4.3.1 Reliability and Failure Distributions	171
4.3.2 Failure Models	175
4.4 Failure Rates and Acceleration Factors	180
4.4.1 Temperature Acceleration	182
4.4.2 Voltage Acceleration	182
4.4.3 Humidity Acceleration	182
4.4.4 ΔT Acceleration	183
4.4.5 Corrosion Models	184
4.5 Acceleration Factors for Multiple Failure Mechanisms	185
4.6 The Impact of Assumed Model Parameters on Reliability Prediction	189
4.7 System Failure Rate Models	191
4.8 Case Studies of Reliability Evaluation for Electronic Packages	193
4.8.1 Reliability Study of Copper Bumps	194
4.8.2 Reliability Study of Flip Chip Modules	196
4.8.3 MAP BGA Reliability Study	196
4.9 Bibliography	197
Appendix: Review of Existing Reliability Simulation Tools	221
A1 Introduction	221
A2 Degradation-Based Reliability Simulation Tools	222
A2.1 Hot Carrier Reliability Simulation in Virtuoso UltraSim	222
A2.2 Hot Carrier Reliability Simulation in Eldo	223
A3 Failure Mechanism Equivalent Circuits	225
A3.1 HCI	226
A3.2 NBTI	232
A3.3 TDDB	234
A4 Failure-Rate-Based SPICE (FaRBS) Simulator	245
A4.1 Assumptions of the FaRBS Model	245
A5 Bibliography	250

List of Figures

	<u>Page</u>
Figure 1: Failure Rate Curve	16
Figure 2: Failure Rates From the ALT	45
Figure 3: The Values of Failure Rates Obtained in the Case Study	47
Figure 4: Traditional Method for Voltage Factor Estimation (C)	48
Figure 5: Estimation of E_a	49
Figure 6: Estimation of Voltage Acceleration Factor γ_2 (HCI).....	51
Figure 7: Estimation of E_{a3} (EM).....	52
Figure 8: Flowchart of the physics-of-failure based statistical reliability estimation method.....	68
Figure 9: Tunneling mechanisms allowing charge to pass the oxide	88
Figure 10: Formation of the traps in the dielectric, creation of conduction path, increased traps and finally the cross section after hard breakdown.....	88
Figure 11: Lifetime extrapolations based on the linear E and 1/E models shows the large discrepancies at the lower electric fields, both models are the same for electric field above 9MV/cm for the field acceleration values [Reference 2]	90
Figure 12: CHE injection involves propelling of carriers in the channel toward the oxide even before they reach the drain area	97
Figure 13: DAHC injection involves impact ionization of carriers near the drain area	99
Figure 14: SHE injection involves trapping of carriers from the substrate.	99
Figure 15: SGHE injection involves hot carriers generated by secondary carriers	100
Figure 16: Lucky electron model.....	101
Figure 17: Cross section of MOSFET structures: (a) As-P(n ⁺ -n ⁻) double diffusion, (b) P-drain, (c) Offset gate, (d)Buried channel	106
Figure 18: Schematic two-dimensional representation of the Si- SiO ₂ interface, showing (a) the $\equiv Si$ defect, (b) how this defect may be electrically activated during NBTI to form an interface trap, a fixed oxide charge, and a hydroxyl group, and (c) the OH diffusion through the oxide [Reference 41]	111
Figure 19: EM Failure Mechanism.....	116

List of Figures (continued)

	<u>Page</u>
Figure 20: Lattice Diffusion, Grain Boundary Diffusion, and Surface Diffusion of Polycrystalline Aluminum	116
Figure 21: Memory Cell Model of Soft Error	119
Figure 22: Complex FC-LGA packages using flip chip as interconnects .	128
Figure 23: The detail structure view of die and the substrate.....	128
Figure 24: Defect driven cracking in the thin film layers of the die	136
Figure 25: Wire Bonding Structures.....	140
Figure 26: Die cracking failures seen in the field application.....	142
Figure 27: Thin film delamination/die cracking failure	142
Figure 28: An example of an interface delamination failure seen in the package	146
Figure 29: Delamination at the ILD after moisture sensitivity level (MSL) testing.....	146
Figure 30: Die cracking failure seen after 600 cycles AATC (die corner delamination failures).....	151
Figure 31: Pass and failed solder joints after thermal cycling test	155
Figure 32: Diagram showing the bumps under electromigration tests	163
Figure 33: Solder joint cracking due to electromigration loads	164
Figure A.1: Hot carrier reliability simulation flowchart in Virtuoso UltraSim [Reference 5].....	223
Figure A.2: HCI reliability simulation in Eldo. A large number of SPICE simulation iterations have to be carried out to obtain accuracy.	225
Figure A.3: BERT n-MOSFET HCI circuit model. (a) Bidirectional interface trap generation near both drain and source. L_f and L_r represent forward and reverse hot carrier damaged regions. (b) HCI drain current ΔI_d circuit model [Reference 8].	227
Figure A.4: UIUC n-MOSFET HCI two-transistor series model. (a) Triangular oxide charge distribution profile used in model derivation. (b) Cross-sectional view of n-MOSFET with hot carrier damage, L_2 is damaged channel region. (c) Two-transistor series circuit model. The parasitic transistor has different channel mobility and threshold voltage with the channel length L_2 set to $0.1\mu m$ [References 11, 13, 14].	228

List of Figures (continued)

	<u>Page</u>
Figure A.5: HCI circuit model in MaCRO. In the model: $V_{gdx}=V_{gs}-V_t-V_{ds}$ and $V_{Rd}=I_{ds} \Delta R_d$. V_t is threshold voltage and I_{ds} is the current from node D to S	230
Figure A.6: MaCRO NBTI circuit model. NBTI-induced p-MOSFET threshold voltage increase is modeled as absolute gate-to-source voltage decrease. Gate tunneling current flowing through the gate resistance R_G leads to the increase of voltage at point G' . This corresponds to the decrease of p-MOSFET absolute gate-to-source voltage and therefore mimics the threshold voltage degradation effect. Gate tunneling current is modeled with two voltage controlled current sources which follow the form of a power law relation as: $I=KV^p$	233
Figure A.7: Power-law leakage current model. The exponent p varies from 5 to 2 as the degradation level increases. K reflects the “size” of the breakdown spot.	235
Figure A.8: TDDDB GOS model for gate-to-channel breakdown of n-MOSFET with n^+ -poly gate. The channel lengths of nMOS ₁ and nMOS ₂ follow the relation: $L_1+L_2=L$ where L is the undamaged n-MOSFET channel length. The parameter R_{GOS} is related to the size and location of the breakdown path. A value of R_{GOS} as low as 3 K Ω was used in the simulation in [Reference 26].	237
Figure A.9: TDDDB RF equivalent circuit model. Model parameters for simulation in Reference 28 are set as: $R_G=85.4 \Omega$, $R_D=R_S=12.14 \Omega$, $R_{GD}=6.88 \text{ K}\Omega$, $R_{GS}=23 \text{ K}\Omega$, $C_{GDO}=C_{GSO}=15.3 \text{ fF}$, $C_{jDB}=C_{jSB}=7 \text{ fF}$, $R_{DSB}=80 \text{ K}\Omega$, $R_{DB}=R_{SB}=49.37 \Omega$	238
Figure A.11: TDDDB circuit model for n-MOSFET with hard gate oxide breakdown and operated in positive gate voltage. (a) Cross-sectional view of breakdown structure. (b) Equivalent circuit model. Model parameters for simulation in are set as: $R_G=1 \text{ K}\Omega$, $L_{M_s} + L_{M_d} =0.09 \mu\text{m}$, $W_{M_s} = W_{M_d} =0.25 \mu\text{m}$, R_D and R_S vary from 2.5 K Ω (at source and drain) to 12.5 K Ω (at the middle of the channel).	240
Figure A.11: MaCRO TDDDB circuit model for n-MOSFET with hard gate oxide breakdown. $I_{OX}=I_S-I_D$ is a voltage dependent current source representing breakdown path current injection effect. R_D and R_S characterize the resistance in the source and the drain extensions, respectively. L_1 represents breakdown location away from the source edge.	243
Figure A.12: Flow chart of the failure rate-based simulation process.....	248

List of Tables

	<u>Page</u>
Table 1: Electronic Reliability Prediction Tool Comparator.....	12
Table 2: Comparison Between MIL-HDBK-217 and Physics-of-Failure...	13
Table 3: Relationship Among Measures	15
Table 4: Examples of Reliability Testing Conducted When New Products are Developed.....	23
Table 5: Classification of Test Standards	23
Table 6: Reliability Test Standard.....	26
Table 7: Typical Example of Accelerated Lifetime Tests.....	28
Table 8: Frequently Used Acceleration Models, Their Parameters and Applications.....	29
Table 9: Definitions of Some of the Terms Used to Describe the Failure Rate of Semiconductor Devices	38
Table 10: The Traditional Test Conditions under High Voltages and High Temperature.....	48
Table 11: The Traditional Test Conditions under High Voltage and Low Temperatures	49
Table 12: Failure Rate with Fixed Low Temperature and High Voltages (HCI).....	51
Table 13: Failure rate with fixed low temperature and high voltages	52
Table 14: The relation among failure modes, mechanisms and factors	84
Table 15: The basic concept of scaling	85
Table 16: Degradation mechanisms for three types of MOSFETs and three stress gate voltage ranges	104
Table 18: Example of field return failures (Parts qualified but failed in the field).....	131
Table 19: Standard stress test types used in electronic package study [JEDEC, 2004/2005/2006]	132
Table 20: Failure Mechanisms Seen in Electronic Packages	135
Table 21: Failure mechanisms seen in BGA packages.....	137
Table 22: Some typical corrosion models	171
Table 23: Beta (β) value of Weibull distribution for some failure mechanisms	174
Table 24: Exponent parameters used in Coffin-Manson models	176

List of Tables (continued)

	<u>Page</u>
Table 25: Failure Mechanisms and Activation Energy (E_a) Obtained	177
Table 26: Models to complex products [Reference 86]	185
Table 27: Experiment matrix of the solder joint study	189
Table 28: Characterization life and shape parameters for the solder joint reliability study	189
Table 29: Model parameters from literatures	190
Table 30: Acceleration factors calculated using the available parameters.	190
Table 31: Weibull parameters for different packages under the same TC condition	191
Table 32: Failure summary of Reliability of Copper Bumps	195
Table 33: Failure summary of reliability study of the flip chip modules...	196
Table 34: Failure summary of reliability study of PBGA Packages	197